AMENDMENT TO THE CLAIMS

1. (Original) An apparatus, comprising:

a phase detector adapted to determine a phase difference between at least two input signals;

a first circuit adapted to generate a control signal based upon the determined phase difference; and

a second circuit adapted to:

receive a first signal;

receive a second signal;

modify the second signal based upon the control signal; and

provide the first signal and the modified second signal as input signals to the phase detector.

2. (Previously Amended) The apparatus of claim 1, wherein the second circuit is adapted to modify the first signal before providing the modified first signal to the phase detector.

3. (Previously Amended) The apparatus of claim 2, wherein the second circuit is adapted to provide the modified first signal and the modified second signal as input signals to the phase detector, and wherein the phase detector is adapted to determine a phase difference between the modified first signal and the modified second signal.

4. (Original) The apparatus of claim 1, wherein the second circuit comprises a fixed delay and an adjustable delay.

5. (Original) The apparatus of claim 4, wherein the fixed delay comprises at least one delay element.

6. (Original) The apparatus of claim 4, wherein the adjustable delay comprises at least two delay elements, at least one of the delay elements in the adjustable delay being selectable based upon the control signal.

7. (Original) The apparatus of claim 1, wherein the phase detector is capable of providing a signal indicative of the determined phase difference to the first circuit.

8. (Previously Amended) The apparatus of claim 7, wherein the signal indicative of the determined phase difference is a binary signal.

9. (Original) The apparatus of claim 8, wherein the control signal is a binary control signal formed using the binary phase difference signal.

10. (Original) The apparatus of claim 1, wherein the first circuit is adapted to provide a signal indicative of a desired clock signal delay based upon the determined phase difference.

11. (Original) The apparatus of claim 1, wherein the first circuit is a majority filter adapted to provide a signal indicative of the desired clock signal delay in response to at least two consecutive determined phase differences in the same direction.

12. (Original) The apparatus of claim 1, wherein the phase detector is at least one of a latch-type detector, an arbiter-type detector, and a counter-type detector.

13. (Original) The apparatus of claim 1, wherein the second circuit comprises a hysteresis adjuster.

14. – 44. (Cancelled).